9. 3D Packaging Failure Analysis - Failure Mechanisms and Analytical Tools

Course Leader: Deepak Goyal – Independent Consultant

Course Description:
Heterogeneous Integration (HI) of disparate computing and communications functions is a key enabler of performance in micro-electronic systems. HI is crucially enabled by advanced packaging since packages are an optimal HI platform. This technical course will provide an overview of the failure modes and mechanisms observed in 2.5D/3D packages. A brief introduction to the methodology of failure analysis of these packages will be described. The focus of the course will be on package failure mechanisms highlighted by case studies and on analytical tools and techniques currently used and the future direction for the tools and techniques required for successful and timely failure analysis of 3D package technologies. A discussion on the strategies for use of these techniques and a flow chart for failure analysis will be included.

Course Outline:

1. 2.5D/3D Package Technology – Trends, Drivers & Challenges
2. Failure Analysis Challenges Offered by 3D Package Technology Roadmap
3. Introduction to the Methodology of Failure Analysis of 3D Packages
4. Current Analytical Capabilities for Package Fault Isolation and Failure Analysis
5. Strategies to use these Techniques to Identify Failures and Understand Failure Mechanisms
6. Analytical Capabilities to Support Next Generation 3D Packaging Technologies
7. Typical Failure Analysis Flow Charts for Opens and Shorts.
8. Failure Modes/mechanisms Including Chip/package Interactions, 1st/2nd Level Interconnections and Package/board Substrates.
9. Failure Analysis Case Studies.

Who Should Attend:
Engineers and technical managers who are involved in package technology development, assembly manufacturing, reliability assessment of packages and failure analysis will benefit from this course.

Bio: Deepak Goyal graduated with a PhD from State University of New York, Stony Brook. He has recently retired as Sr. PE leading the Assembly and Test Technology Development Failure Analysis Labs at Intel. His responsibilities included defect characterization, fault isolation, yield, failure and materials analyses for the next generation package technology development at Intel; analytical chemistry labs in support of the substrate development and manufacturing, and Board and System level failure analysis; and development of the next generation of analytical metrologies, tools and techniques. He has helped with the development of all Intel assembly technologies including FCxGA, FCCSP, TSVs, POINT, EMIB and Foveros. He is an expert in the defect characterization and failure analysis of packages and has taught Professional Development courses on Package FA/FI methods and failure mechanisms at the Electronics Components and Technology Conference (ECTC). Deepak has authored and co-authored over 50 papers and holds 19 US patents. He has co-authored 2 book chapters and has co-edited 2 books on “3D Microelectronic Packaging”. He is an IEEE Fellow.